## REMARKS

Claims 1-10 were examined and reported in the Office Action. Claims 1-10 are rejected. Claims 1, 4, 7 and 9 are amended. Claims 1-10 remain.

Applicant requests reconsideration of the application in view of the following remarks.

## I. 35 U.S.C. § 103(a)

It is asserted in the Office Action that claims 1-10 are rejected in the Office Action under 35 U.S.C. § 103(a), as being unpatentable over U. S. Patent No. 5,802,080 issued to Westby ("Westby") in view of U. S. Patent No. 6,393,489 issued to Sambamurthy ("Sambamurthy "). Applicant traverses the aforementioned rejection for the following reasons.

According to MPEP §2142

> [t]o establish a prima facie case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure." (In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991)).

Further, according to MPEP §2143.03, "[t]o establish prima facie obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. (In re Royka, 490 F.2d 981, 180 USPQ 580 (CCPA 1974). "*All words in a claim must be considered* in judging the patentability of that claim against the prior art." (In re Wilson, 424 F.2d 1382, 1385, 165 USPQ 494, 496 (CCPA 1970), emphasis added.)

Applicant's claim 1 contains the limitation of

> [a] cyclic redundancy check (CRC) verification apparatus having constant delay, ...a CRC generation unit which ... generates information on a write address which increases sequentially irrespective of the input of the data frame, ... and provides a read address synchronization signal that makes a read address follows with a predetermined offset after the write address; and an output control unit which receives the read address synchronization signal, generates the read address which increases sequentially, sends the read address to the data buffer and the control information buffer, reads data stored in the data buffer, and outputs a different output control signal together with the data according to the CRC result, wherein the CRC verification apparatus receives input frames at a constant rate irrespective of a received data frame while CRC verification is performed.

Applicant's amended claim 4 contains the limitations of

> [a] CRC verification apparatus having constant delay, comprising: ... a CRC generation unit which ... generates information on a write address which increases sequentially irrespective of the input of the data frame, ... and provides a read address synchronization signal that makes a read address follows with a predetermined offset after the write address; and an output control unit which receives the read address synchronization signal, generates the read address which increases sequentially, sends the read address information to the buffer, reads data stored in the buffer, and outputs a different output control signal together with the data according to the CRC result, wherein the CRC verification apparatus receives input frames at a constant rate irrespective of a received data frame while CRC verification is performed.

Applicant's amended claim 7 contains the limitations of

> [a] CRC verification apparatus having constant delay, comprising: ...an output control unit which with a predetermined offset from the write address, reads the input data frames and if the CRC verification result is normal, output the read data frame, wherein the CRC verification apparatus receives input frames at a constant rate irrespective of a received data frame while CRC verification is performed.

Applicant's amended claim 9 contains the limitations of

> [a] CRC verification method having constant delay, comprising: ... generating a CRC enable signal, generating write address which

> increases sequentially irrespective of the input of the data frame, ... and providing a read address synchronization signal that makes the read address follow with a predetermined offset after the write address; ...generating information on a read address which increases sequentially, ..., wherein input frames are received at a constant rate irrespective of received data frames while the CRC verification is performed.

Westby discloses using cyclic redundancy check (CRC) generator as a CRC checker to verify received CRC data in a multi-port system. Westby further discloses that only one CRC generator is used when plural ports receive data. Westby, however, does not teach, disclose or suggest Applicant's claim 1 limitations of:

> [a] cyclic redundancy check (CRC) verification apparatus having constant delay, ...a CRC generation unit which ... generates information on a write address which increases sequentially irrespective of the input of the data frame, ... and provides a read address synchronization signal that makes a read address follows with a predetermined offset after the write address; and an output control unit which receives the read address synchronization signal, generates the read address which increases sequentially, ... wherein the CRC verification apparatus receives input frames at a constant rate irrespective of a received data frame while CRC verification is performed;

Applicant's claim 4 limitations of:

> a CRC generation unit which ... generates information on a write address which increases sequentially irrespective of the input of the data frame, ... and provides a read address synchronization signal that makes a read address follows with a predetermined offset after the write address; and an output control unit which ... generates the read address which increases sequentially, sends the read address information to the buffer, ... wherein the CRC verification apparatus receives input frames at a constant rate irrespective of a received data frame while CRC verification is performed;

Applicant's claim 7 limitations of:

> [a] CRC verification apparatus having constant delay, comprising: ...an output control unit which with a predetermined offset from the write address, ... wherein the CRC verification apparatus receives input frames at a constant rate irrespective of a received data frame while CRC verification is performed;

nor Applicant's claim 9 limitations of:

> [a] CRC verification method having constant delay, comprising: ... generating a CRC enable signal, generating write address which increases sequentially irrespective of the input of the data frame, ... and providing a read address synchronization signal that makes the read address follow with a predetermined offset after the write address; and receiving the read address synchronization signal, generating information on a read address which increases sequentially, reading the stored data frame according to this read address information, and according to the CRC result, outputting a different output control signal together with the output data, wherein input frames are received at a constant rate irrespective of received data frames while the CRC verification is performed.

Sambamurthy discloses integrated circuits for processing and managing flow of data in high speed networks. It is asserted in the Office Action that Sambamurthy discloses "an output control unit which with a predetermined offset from the write address, reads the input data frames and if the CRC verification result is normal, output the read data frame." The description relied on in Sambamurthy relates to "appropriate processing," which may include pad stripping, start sample line, self receive and receive enable operations. (Sambamurthy, column 27, lines 30-41). Data packet processing as described in Sambamurthy does not teach, disclose or suggest "an output control unit which with a predetermined offset from the write address, reads the input data frames and if the CRC verification result is normal, output the read data frame, wherein the CRC verification apparatus receives input frames at a constant rate irrespective of a received data frame while CRC verification is performed."

Neither Westby, Sambamurthy, and therefore, nor the combination of the two, teach, disclose or suggest the limitations contained in Applicant's amended claims 1, 4, 7 and 9, as listed above. Since neither Westby, Sambamurthy, and therefore, nor the combination of the two, teach, disclose or suggest all the limitations of Applicant's amended claims 1, 4, 7 and 9, Applicant's amended claims 1, 4, 7 and 9 are not obvious over Westby in view of Sambamurthy since a *prima facie* case of obviousness has not been met under MPEP §2142. Additionally, the claims that directly or indirectly depend from amended claims 1, 4, 7 and 9, namely claims 2-3,

5-6, 8, and 10, respectively, would also not be obvious over Westby in view of Sambamurthy for the same reason.

Accordingly, withdrawal of the 35 U.S.C. § 103(a) rejections for claims 1-10 is respectfully requested.

## CONCLUSION

In view of the foregoing, it is submitted that claims 1-10 patentably define the subject invention over the cited references of record, and are in condition for allowance and such action is earnestly solicited at the earliest possible date. If the Examiner believes a telephone conference would be useful in moving the case forward, he is encouraged to contact the undersigned at (310) 207-3800.

If necessary, the Commissioner is hereby authorized in this, concurrent and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2666 for any additional fees required under 37 C.F.R. §§1.16 or 1.17, particularly, extension of time fees.

Respectfully submitted,

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Dated: August 31, 2006

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**CERTIFICATE OF MAILING**

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail with sufficient postage in an envelope addressed to: Mail Stop Amendment, Commissioner for Patents, P. O. Box 1450, Alexandria, Virginia 22313-1450 on August 31, 2006.

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Jean Svoboda